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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/825,426	04/16/2004	Han Sang Lee	8733.1033.00-US	9939
30827	7590	11/24/2009		
MCKENNA LONG & ALDRIDGE LLP 1900 K STREET, NW WASHINGTON, DC 20006			EXAMINER MA, CALVIN	
			ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/825,426	Applicant(s) LEE ET AL.	
	Examiner CALVIN C. MA	Art Unit 2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 August 2009.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-7 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-7 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Komiya US Pub: 2002/0158587 in view of in view of Kochevar (US Patent: 2890332).

As to claim 1, Komiya (Fig. 5) teaches an electro-luminescence (EL) display, include:

a plurality of drive voltage supply lines (e.g., plurality power lines connected to each of pixel in vertical direction from power source PVDD);

a plurality of compensation voltage supply lines (e.g., lines connect to VEE);

EL cells (EL) at each crossing of a plurality of data lines and a plurality of gate lines in a matrix (see Fig. 5), wherein the EL cells emit light in response to currents applied from the drive voltage supply lines (e.g., when TFT2 is on, an electrical current flows from source PVDD into EL; see [0034]).

driving thin film transistors (TFT2) connected between the EL cells and compensation voltage supply lines that control the current applied to the EL cells;

connection between N-1 th compensation voltage supply line (e.g., second VEE line) and a control terminal of the driving TFT and a control terminal of the driving TFT (e.g., TFT2) connected to the Nth compensation voltage (e.g., VEE line of second row), to apply a voltage to the driving TFT connected to the Nth compensation voltage supply line (e.g., TFT2) when a scan pulse is supplied to the N-1 th gate line, wherein the bias switch is controlled by the scan pulse supplied to the N-1 gate line (e.g., gate line 1, see Fig. 5).

However Komiya does not teach a bias switch but rather uses a conventional switch to operate the compensation mechanism between the adjacent gate lines and the pixel structures (see Fig. 5), Kochevar teaches a bias switch as a function circuit component having the capability to be adapted by any electric system (i.e. the demonstration of the working parameter of the bias switch and its implementation within a display system as a complete component) (see Kochevar Fig. 1, Col. 1, Lines 15-45).

Therefore it would have been obvious for one of ordinary skill in the art at the time the invention was made to have used the bias control circuitry of Kochevar to control the switching circuitry in Komiya (i.e. the bias switch for the N-1 line where bias voltage is applied to the EL circuit) in order to expand the possibility of circuitry implementation of applying biased voltage control(see Kochevar Col. 1, Lines 15-45).

As to claim 2, Komiya teaches a switching thin film transistor (TFT1), connected to the gate line (e.g., Discharge gate line 2), the data line (e.g., data line 1) and the

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control terminal of the driving TFT (e.g., TFT4); and
a storage capacitor connected between the compensation voltage supply line (e.g., VEE line) and the control terminal of the driving TFT (e.g., TFT 2).

As to claim 3, Komiya and Kochevar teaches wherein the bias switch (Okuda 31) includes a control terminal connected to the N-1 th gate line (e.g., gate line 1); a first input terminal connected to the N-1 th compensation voltage supply line (e.g., the first top VEE); and

a second input terminal connected to the control terminal of the driving TFT that is connected to the Nth compensation voltage supply line (e.g., the bias switch 31 is connected to the next gate line which reside between the two neighboring cell) (see Komiya, Fig. 5, [0043], [0044]).

3. Claims 4-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Komiya in view of Kochevar as applied in claims 1-3, further in view of Morosawa US Pub: 2006/0139251.

As to claim 4, note the discussion claim 1 above, Komiya and Kochevar teaches plurality of compensation voltage supply lines. Komiya do not teaches a compensation voltage generator that generates a compensation voltage with a high state; and

a shift register that sequentially shifts the compensation voltage with a high state to supply the compensation voltage. Morosawa teaches a voltage generator (140) that

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generates a voltage with a high state (see [0130]); and a shift register (131 b) that sequentially shifts the compensation voltage with a high state (see [0130]).

Therefore, it would have been obvious to one of ordinary skill in the art at time the invention was made to have provided with a voltage generator that generates a compensation voltage with a high state; and a shift register that sequentially shifts the voltage with a high state to supply the voltage as taught by Morosawa to the compensation voltage lines of the organic el pixel circuit of Komiya because the shift register of Morosawa would reduce the amount of time required for generation of the drive current, thereby improving the display image quality (see [0012]).

As to claim 5, Morosawa teaches a high state (e.g., high voltage supply, see [0087]) from the shift register and a low state from the shift register (e.g., the clock from the shift register control the data line and each potential set as low potential state, see [0097], [0326]).

As to claim 6, Komiya teaches wherein the scan pulse is supplied to the N-1th gate line (e.g., gate line 2, see Fig. 5), the control terminal of the driving TFT (e.g., TFT4) is supplied with data (e.g., data line 1) via the switching TFT and the second input terminal is supplied with a compensation voltage (e.g., VEE from the N-1th compensation voltage supply line). Komiya does not teach a low state. Morosawa teaches low state (see [0097]). Therefore, the combination of Komiya, Okuda and

Morosawa meets the claimed limitation.

As to claim 7, Komiya and Kochevar teaches wherein when the scan pulse is supplied to the N-1 th gate line (e.g., gate line 1), the bias switch (e.g., 31) supplies a compensation voltage (e.g., VEE at the top) from the N-1 th compensation voltage supply line to the control terminal of the driving TFT (TFT4 below from gate line 2) connected to the Nth compensation voltage supply line and a compensation voltage is supplied from the Nth (e.g., VEE below from gate line) compensation voltage supply line to the second input terminal of the driving TFT (see Fig. 5). Komiya does not teach low state and high state. Morosawa teaches low state and high state (see [0097] and [0087] respectively). Therefore the combination of Komiya, Okuda and Morosawa meet's the claimed limitation.

Response to Arguments

4. Applicant's arguments filed 8/19/2009 have been fully considered but they are not persuasive.

Regarding the applicant's argument with respect to claims 1-7, the examiner in the new office action did not use the prior art Okuda and therefore the argument with respect to Okuda is moot.

Also the applicant argues in page 11 of the response that the bias switch of Kochevar is not analogous because it is applied in a cathode ray tube, the examiner disagrees because Kochevar's disclosure though made regarding an earlier technology

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attempts to solve the same type of display controlling problem where a bias switch being a fundamental electronic components are able to function in the display field with the same result, since in this case Kochevar is used to show that an artisan at the time of the invention can user bias switching in place of the normal switching system of Komiya's TFT3 components to reduce negative effects such as transient surges, therefore the concept of the bias switch is combined with the modern TFT transistor design to provide the same type of circuitry construct. Therefore the additional bias switching capability of Kochevar in view of the N, N-1 control based system of Komiya still read on the broadest interpretation of the independent claims.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Calvin Ma whose telephone number is (571)270-1713.

The examiner can normally be reached on Monday-Friday, 8:00:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh Nguyen can be reached on 571 272 7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Calvin Ma
November 18, 2009

/Chanh Nguyen/
Supervisory Patent Examiner, Art
Unit 2629